DI LC²MOS Precision Quad SPST Switches

ADG411/ADG412/ADG413

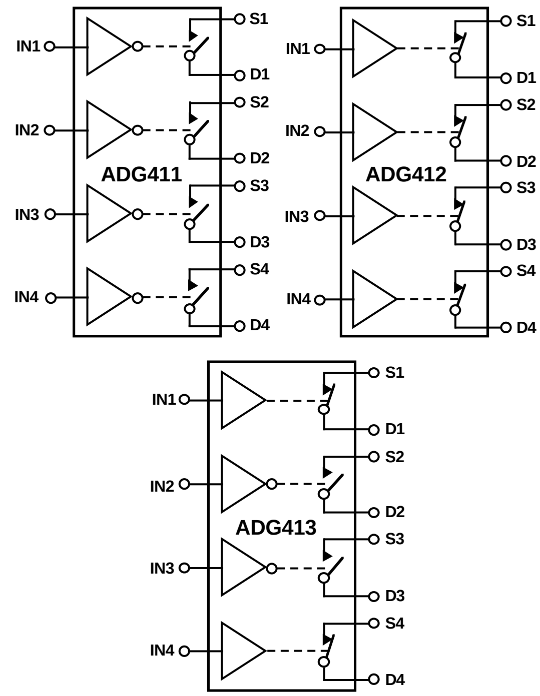
FEATURES

44 V Supply Maximum Ratings
±15 V Analog Signal Range
Low On Resistance (<35 Ω)
Ultralow Power Dissipation (35 μW)
Fast Switching Times
t_{ON} <175 ns
t_{OFF} <145 ns
Latch-Up Proof
TTL/CMOS Compatible
Plug-In Replacement for DG411/DG412/DG413

APPLICATIONS

Audio and Video Switching
Automatic Test Equipment
Precision Data Acquisition
Battery Powered Systems
Sample Hold Systems
Communication Systems

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG411, ADG412 and ADG413 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS, trench isolated process which provides low power dissipation yet gives high switching speed and low on resistance. Trench isolation gives all the benefits of dielectric isolation and ensures no latch up even under extreme overvoltage conditions.

The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals. Fast switching speed coupled with high signal bandwidth also make the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

The ADG411, ADG412 and ADG413 contain four independent SPST switches. The ADG411 and ADG412 differ only in that the digital control logic is inverted. The ADG411 switches are turned on with a logic low on the appropriate control input, while a logic high is required for the ADG412. The ADG413 has two switches with digital control logic similar to that of the ADG411 while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break before make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG411, ADG412 and ADG413 are fabricated on an enhanced LC²MOS, trench isolated process giving an increased signal range which extends fully to the supply rails.
2. Ultralow Power Dissipation
3. Low R_{ON}
4. Trench Isolation Guards Against Latch-up
   A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.
5. Break Before Make Switching
   This prevents channel shorting when the switches are configured as a multiplexer.
6. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG411, ADG412 and ADG413 can be operated from a single rail power supply. The parts are fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5 V.

REV. 0

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ADG411/ADG412/ADG413–SPECIFICATIONS[1]

Dual Supply (V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, V_L = +5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{DD} to V_{SS}		V_{DD} to V_{SS}	V	
R_{ON}	25		25		Ω typ	V_D = ±8.5 V, I_S = –10 mA;
	35	45	35	45	Ω max	V_{DD} = +13.5 V, V_{SS} = –13.5 V
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
Source OFF Leakage I_S (OFF)	±0.1		±0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.25	±20	±0.25	±20	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.1		±0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.25	±20	±0.25	±20	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.1		±0.1		nA typ	V_D = V_S = ±15.5 V;
	±0.4	±40	±0.4	±40	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}	0.005		0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5		±0.5	µA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	110		110		ns typ	R_L = 300 Ω, C_L = 35 pF;
		175		175	ns max	V_S = ±10 V; Test Circuit 4
t_{OFF}	100		100		ns typ	R_L = 300 Ω, C_L = 35 pF;
		145		145	ns max	V_S = ±10 V; Test Circuit 4
Break-Before-Make Time Delay, t_D (ADG413 Only)	25		25		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = +10 V; Test Circuit 5
Charge Injection	5		5		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 6
OFF Isolation	68		68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	9		9		pF typ	f = 1 MHz
C_D (OFF)	9		9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		35		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V Digital Inputs = 0 V or 5 V
I_{DD}	0.0001		0.0001		µA typ	
	1	5	1	5	µA max	
I_{SS}	0.0001		0.0001		µ A typ	
	1	5	1	5	µA max	
I_L	0.0001		0.0001		µA typ	
	1	5	1	5	µA max	

NOTES

[1]Temperature ranges are as follows: B Versions: –40°C to +85°C; T Versions: –55°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Single Supply (V_{DD} = +12 V ± 10%, V_{SS} = 0 V, V_L = +5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SIGNAL RANGE		0 V to V_{DD}		0 V to V_{DD}	V	
R_{ON}	40		40		Ω typ	0 < V_D = 8.5 V, I_S = –10 mA;
	80	100	80	100	Ω max	V_{DD} = +10.8 V
LEAKAGE CURRENTS						V_{DD} = +13.2 V
Source OFF Leakage I_S (OFF)	±0.1		±0.1		nA typ	V_D = 12.2/1 V, V_S = 1/12.2 V;
	±0.25	±20	±0.25	±20	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.1		±0.1		nA typ	V_D = 12.2/1 V, V_S = 1/12.2 V;
	±0.25	±20	±0.25	±20	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.1		±0.1		nA typ	V_D = V_S = +12.2 V/+1 V;
	±0.4	±40	±0.4	±40	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}	0.005		0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5		±0.5	µA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	175		175		ns typ	R_L = 300 Ω, C_L = 35 pF;
		250		250	ns max	V_S = +8 V; Test Circuit 4
t_{OFF}	95		95		ns typ	R_L = 300 Ω, C_L = 35 pF;
		125		125	ns max	V_S = +8 V; Test Circuit 4
Break-Before-Make Time Delay, t_D (ADG413 Only)	25		25		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = +10 V; Test Circuit 5
Charge Injection	25		25		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 6
OFF Isolation	68		68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	9		9		pF typ	f = 1 MHz
C_D (OFF)	9		9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		35		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +13.2 V Digital Inputs = 0 V or 5 V
I_{DD}	0.0001		0.0001		µA typ	
	1	5	1	5	µA max	
I_L	0.0001		0.0001		µA typ	
	1	5	1	5	µA max	V_L = +5.25 V

NOTES
[1]Temperature ranges are as follows: B Versions: –40°C to +85°C; T Versions: –55°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

Truth Table (ADG411/ADG412)

ADG411 In	ADG412 In	Switch Condition
0	1	ON
1	0	OFF

Truth Table (ADG413)

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} . . . . +44 V
V_{DD} to GND . . . . –0.3 V to +25 V
V_{SS} to GND . . . . +0.3 V to –25 V
V_L to GND . . . . –0.3 V to V_{DD} + 0.3 V
Analog, Digital Inputs[2] . . . . V_{SS} –2 V to V_{DD} +2 V or 30 mA, Whichever Occurs First
Continuous Current, S or D . . . . 30 mA
Peak Current, S or D . . . . 100 mA
(Pulsed at 1 ms, 10% Duty Cycle max)
Operating Temperature Range
  Industrial (B Version) . . . . –40°C to +85°C
  Extended (T Version) . . . . –55°C to +125°C
Storage Temperature Range . . . . –65°C to +150°C
Junction Temperature . . . . +150°C
Cerdip Package, Power Dissipation . . . . 900 mW
  θ_{JA} Thermal Impedance . . . . 76°C/W
  Lead Temperature, Soldering (10 sec) . . . . +300°C
Plastic Package, Power Dissipation . . . . 470 mW
  θ_{JA} Thermal Impedance . . . . 117°C/W
  Lead Temperature, Soldering (10 sec) . . . . +260°C
SOIC Package, Power Dissipation . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . 77°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . +215°C
    Infrared (15 sec) . . . . +220°C

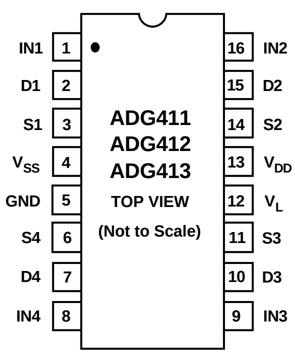
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.
[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG411/ADG412/ADG413 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION (DIP/SOIC)



ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG411BN	–40°C to +85°C	N-16
ADG411BR	–40°C to +85°C	R-16A
ADG411TQ	–55°C to +125°C	Q-16
ADG412BN	–40°C to +85°C	N-16
ADG412BR	–40°C to +85°C	R-16A
ADG412TQ	–55°C to +125°C	Q-16
ADG413BN	–40°C to +85°C	N-16
ADG413BR	–40°C to +85°C	R-16A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.
[2]N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); Q = Cerdip.

TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to GND.
V_L	Logic power supply (+5 V).
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
R_{ON}	Ohmic resistance between D and S.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	"OFF" switch source capacitance.
C_D (OFF)	"OFF" switch drain capacitance.
C_D, C_S (ON)	"ON" switch capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on.
t_{OFF}	Delay between applying the digital control input and the output switching off.
t_D	"OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Typical Performance Graphs

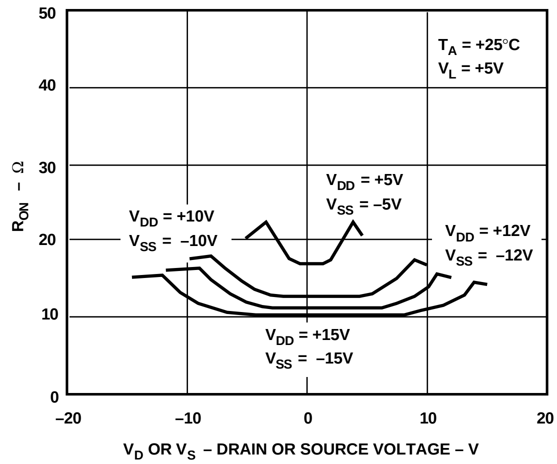


Figure 1. On Resistance as a Function of V_D (V_S) Dual Supplies

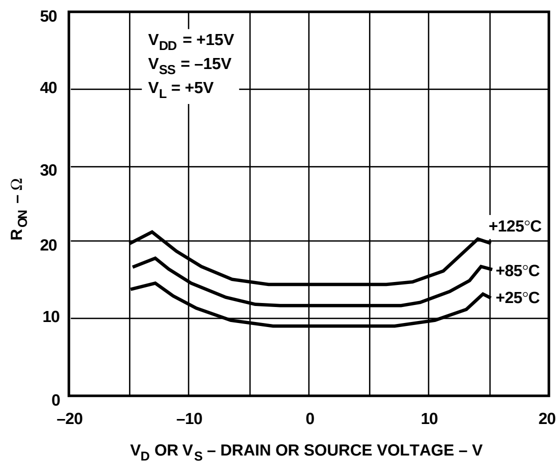


Figure 2. On Resistance as a Function of V_D (V_S) for Different Temperatures

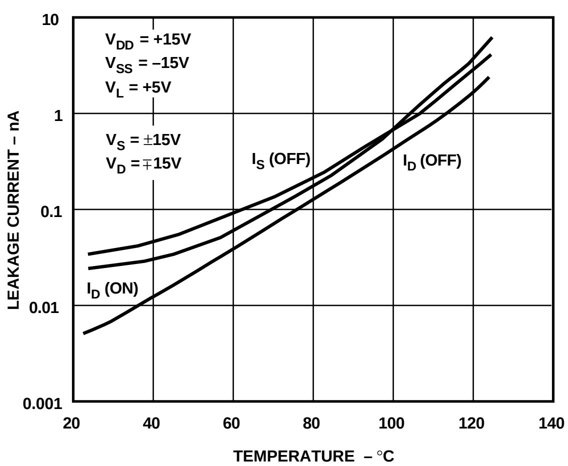


Figure 3. Leakage Currents as a Function of Temperature

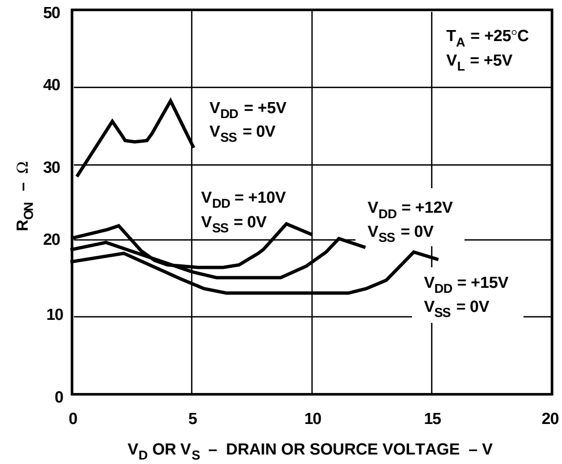


Figure 4. On Resistance as a Function of V_D (V_S) Single Supply

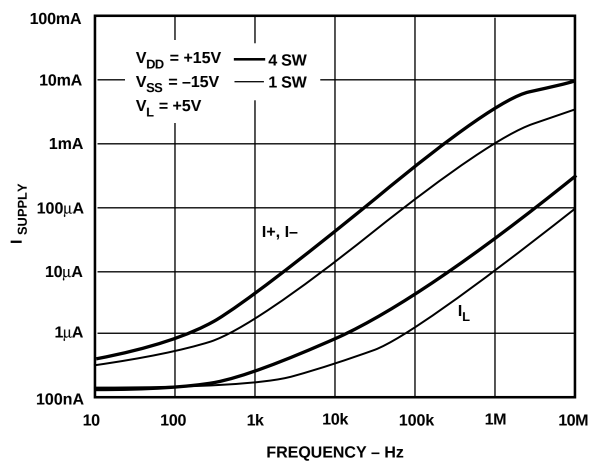


Figure 5. Supply Current vs. Input Switching Frequency

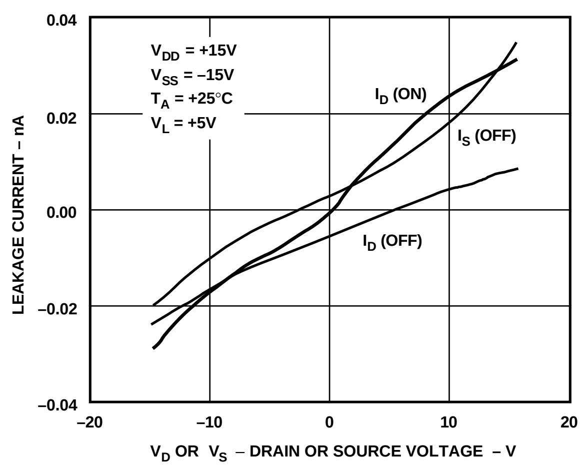


Figure 6. Leakage Currents as a Function of V_D (V_S)

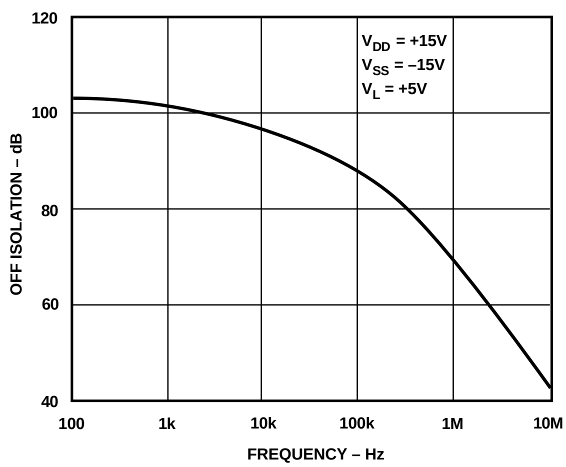


Figure 7. Off Isolation vs. Frequency

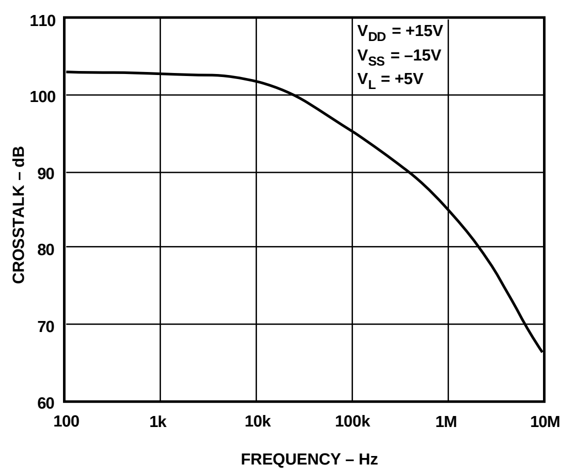


Figure 8. Crosstalk vs. Frequency

TRENCH ISOLATION

In the ADG411, ADG412 and ADG413, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in Junction Isolated switches, are eliminated, the result being a completely latch-up proof switch.

In Junction Isolation, the N and P wells of the PMOS and NMOS transistors form a diode which is reverse-biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. A Silicon-Controlled Rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current which, in turn, leads to latch-up. With Trench Isolation, this diode is removed, the result being a latch-up proof switch.

Trench Isolation also leads to lower leakage currents. The ADG411, ADG412 and ADG413 have a leakage current of 0.25 nA as compared with a leakage current of several nanoamps in non-Trench Isolated switches. Leakage current is an important parameter in sample-and-hold circuits, this current being responsible for the discharge of the holding capacitor with time causing droop. The ADG411/ADG412/ADG413's low leakage current, along with its fast switching speeds, make it suitable for fast and accurate sample-and-hold circuits.

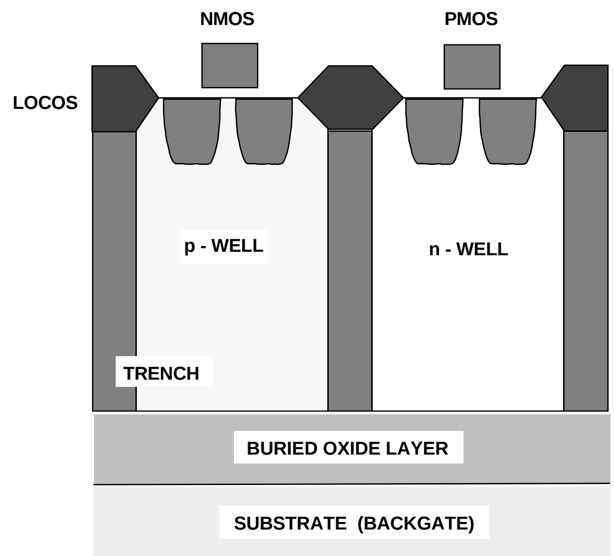


Figure 9. Trench Isolation

APPLICATION

Figure 10 illustrates a precise, fast sample-and-hold circuit. An AD845 is used as the input buffer while the output operational amplifier is an AD711. During the track mode, SW1 is closed and the output V_{OUT} follows the input signal V_{IN}. In the hold mode, SW1 is opened and the signal is held by the hold capacitor C_H.

Due to switch and capacitor leakage, the voltage on the hold capacitor will decrease with time. The ADG411/ADG412/ADG413 minimizes this droop due to its low leakage specifications. The droop rate is further minimized by the use of a polystyrene hold capacitor. The droop rate for the circuit shown is typically 30 µV/µs.

A second switch SW2, which operates in parallel with SW1, is included in this circuit to reduce pedestal error. Since both switches will be at the same potential, they will have a differential effect on the op amp AD711 which will minimize charge injection effects. Pedestal error is also reduced by the compensation network R_C and C_C. This compensation network also reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the ±10 V input range. Both the acquisition and settling times are 850 ns.

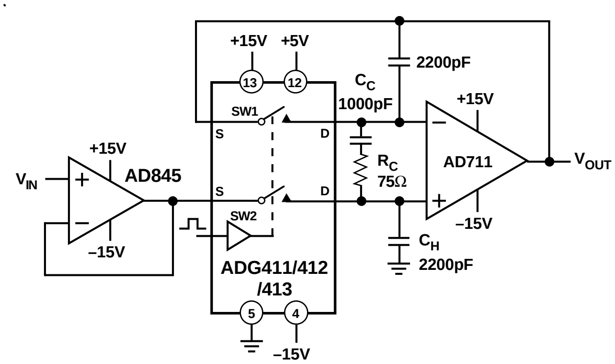
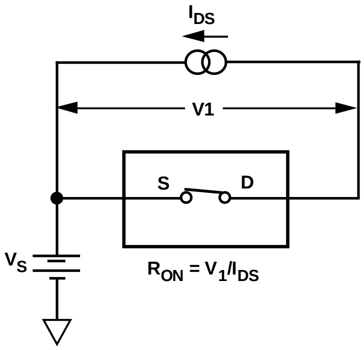
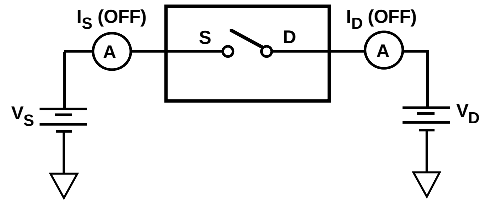


Figure 10. Fast, Accurate Sample-and-Hold

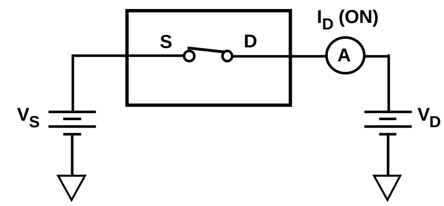
Test Circuits



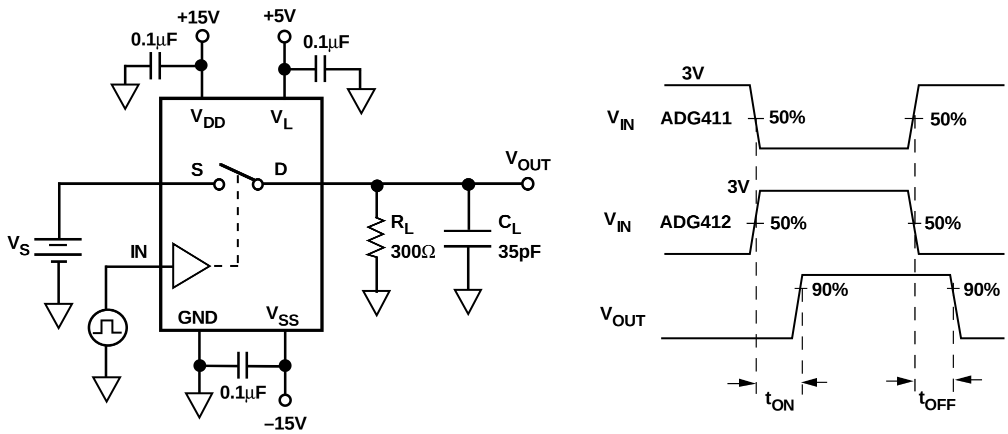
Test Circuit 1. On Resistance



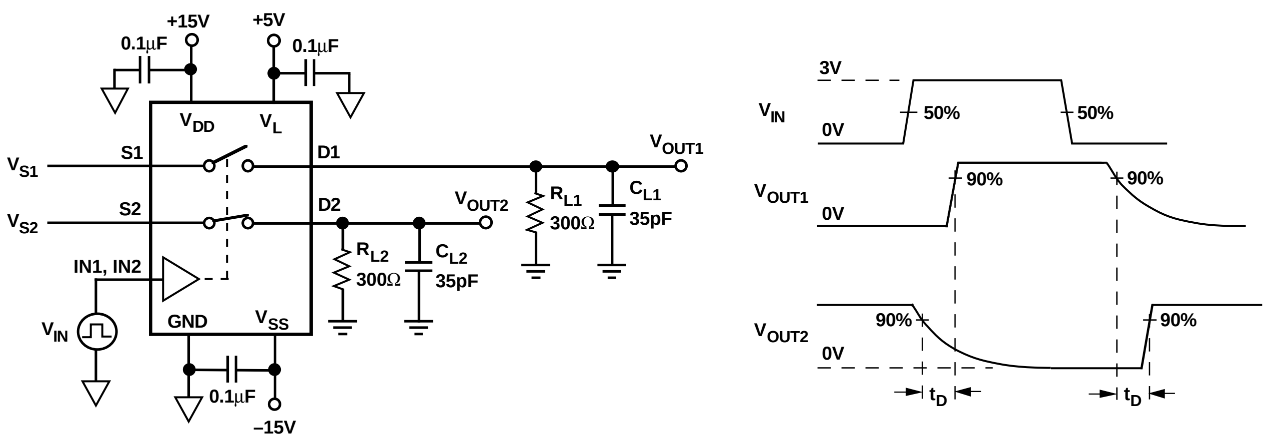
Test Circuit 2. Off Leakage



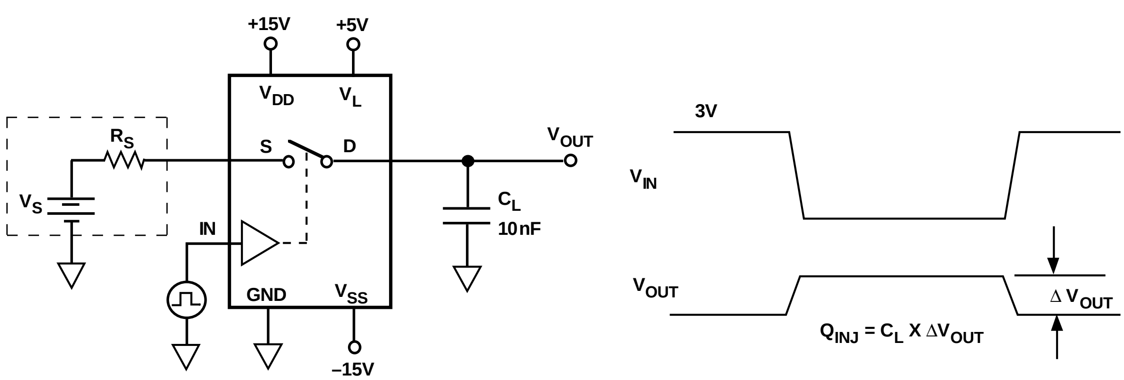
Test Circuit 3. On Leakage



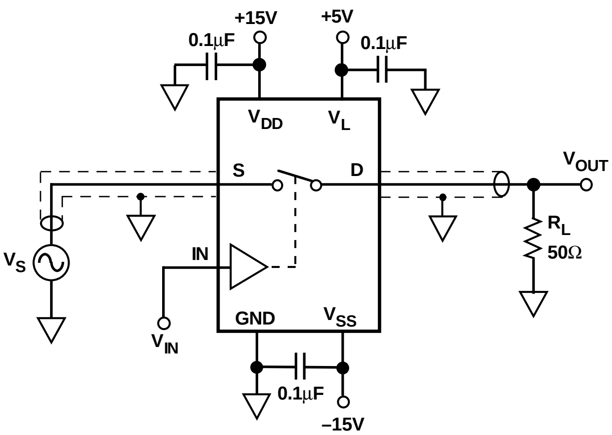
Test Circuit 4. Switching Times



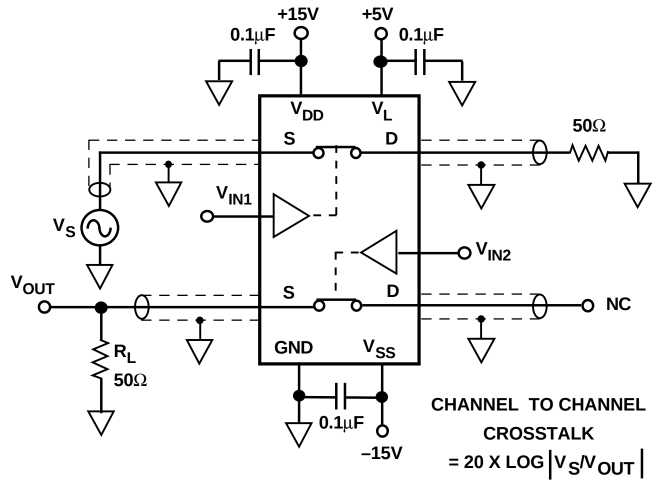
Test Circuit 5. Break-Before-Make Time Delay



Test Circuit 6. Charge Injection



Test Circuit 7. Off Isolation

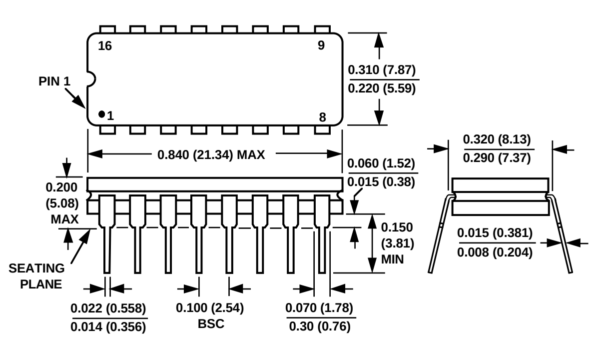


Test Circuit 8. Channel-to-Channel Crosstalk

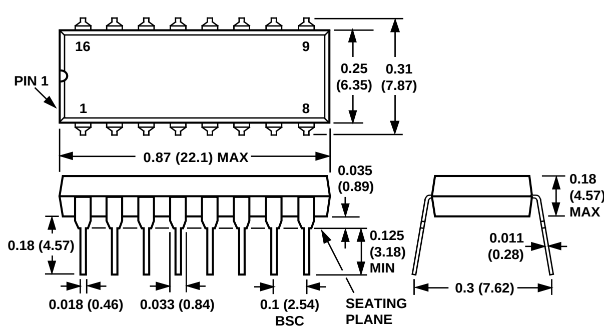
MECHANICAL INFORMATION

Dimensions are shown in inchcs and (mm).

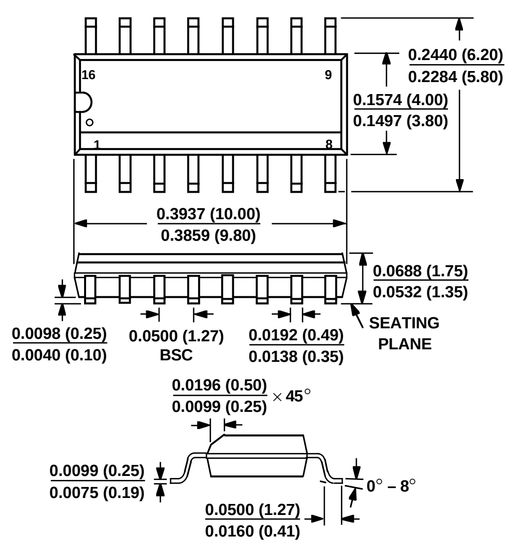
16-Pin Cerdip (Q-16)



16-Pin Plastic DIP (N-16)



16-Pin SOIC (R-16A)



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